longer transparent. In other words, signals will not flow across this path. However, Node A retains its value just prior to the de-assertion event. In the system 200, Div_Select and Node A each are "q" bits wide. Therefore, to

5   accommodate "q" bits, "q" D-latches will be used in parallel, that is, 1 D-latch for each bit.

Synchronizer 1 220 synchronizes Node A with Clk_in such that its outputs d1, d2, … dn are synchronized outputs resulting from this event. Synchronizer 1 220 also has

10 built into it an n to 2^n decoder. For example, if Node A is a 3 bit input, then Synchronizer 1 will generate 8 outputs (d1 to d8) corresponding with 8 different divider settings. The settings will then be inputted into the divider 230. Synchronizer 2 250 synchronizes Node B with Clk_Out such

15 that the out put Node C is a synchronized version (with respect to Clk_Out) of the value at Node B

Synchronizer 1 220 and Synchronizer 2 250 have reset inputs. When reset is asserted then regardless of the states of the other inputs, the outputs of the synchronizers

20 are set to a pre-determined logic value.

In the system 200, the divider takes in Clk_In, and provides a frequency divided version of Clk_In at Clk_Out. The divider has /1_{min} /n settings. These settings are selected by the outputs of Synchronizer 1 220. The divider

25 230 also has a reset input. When reset is asserted, regardless of the current state of the other divider inputs, the divider output, Clk_Out, is set to a predetermined logic value. Further, when the reset to Synchronizer 1 220 is asserted, its outputs d1 … dn are such that they put the

30 output of the Divider Clk_Out to this predetermined logic value. In a further embodiment, the Or gate 260 is employed so that, if necessary, a manual reset can be performed using external reset bypassing all current operations.

● PRINTER RUSH ●
(PTO ASSISTANCE)

Application : 10/809 592	**Examiner :** Wambach	**GAU :** 2816
From: PAP	**Location:** (IDE) FMF FDC	**Date:** 9/13/05

Tracking #: EPM 10/809592   **Week Date:** 6/27/05

DOC CODE	DOC DATE	MISCELLANEOUS
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☐ OATH	_____	
☐ 312	_____	
☑ SPEC	3/25/04	

[RUSH] **MESSAGE:** Page 8, line 23 of the Specification has illegible data. Please advise.

Thank you

[XRUSH] **RESPONSE:** Information is /1.../n

INITIALS: (PAP)

NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.
REV 10/04

Voice